Hardware-Software Co-Design for Security: ECC Processor Example

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SILM Workshop, Nov. 2019

Introduction

Public-key (or asymmetric) cryptography (PKC):

- RSA
- (hyper-)elliptic curve cryptography ((H)ECC)
- post-quantum crypto (PQC)

Design, prototype and evaluate hardware/software (HW/SW) for PKC:

- HW: computation units, accelerators, crypto-processors
- SW: libraries, generators for HW, dedicated compiler for our processors

Objectives:

- high speed, reduced silicon area and energy consumption
- protections against side-channel and fault-injection attacks (SCA/FIA)
- HW: FPGA and ASIC implementations
- SW: embedded processors implementations

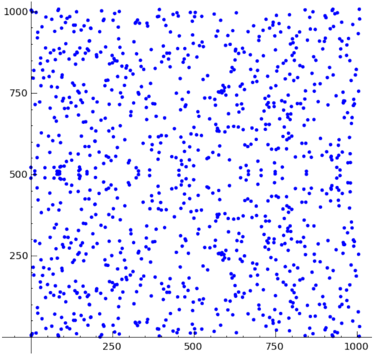
Elliptic Curve Cryptography (ECC)

Elliptic curve over GF(p):

$$E: \quad y^2 = x^3 + ax + b$$

Curve points representation:

- $P = (x, y)$ affine coordinates
  ☹ many field inversions
- $P = (x, y, z, \ldots)$ redundant coordinates
  ☺ significantly faster (e.g., Jacobian)



$y^2 = x^3 + 4x + 20$ over $\mathrm{GF}(1009)$

Scalar multiplication:

$$Q = [k]P = \underbrace{P + P + \cdots + P}_{k \text{ times}}$$

The most time consuming operation in protocols

where $P \in E$ and $k = (k_{n-1}k_{n-2}\ldots k_1k_0)_2$

k has 200–600 bits

Good and complete presentation in [14] and [10]

Scalar Multiplication

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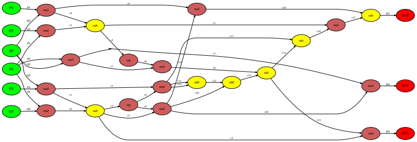
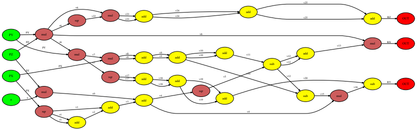
Double-and-add scalar multiplication algorithm:

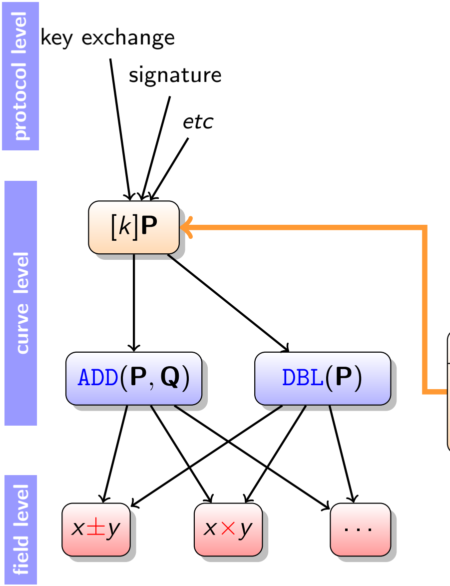
$Q \leftarrow \mathcal{O}$
for i **from** $n-1$ **to** 0 **do**
  $Q \leftarrow [2]Q$ (DBL)
  if $k_i = 1$ **then** $Q \leftarrow Q + P$ (ADD)
return Q

- scans each bit of k and performs corresponding curve-level operation
- average cost: $0.5n$ ADD $+ n$ DBL (security ➔ $\approx 0.5n$ ones in k)





Side Channel Attacks



Scalar multiplication operation

for i from 0 to $t-1$ do
  if $k_i = 1$ then $\mathbf{Q} = \mathtt{ADD}(\mathbf{P}, \mathbf{Q})$
  $\mathbf{P} = \mathtt{DBL}(\mathbf{P})$

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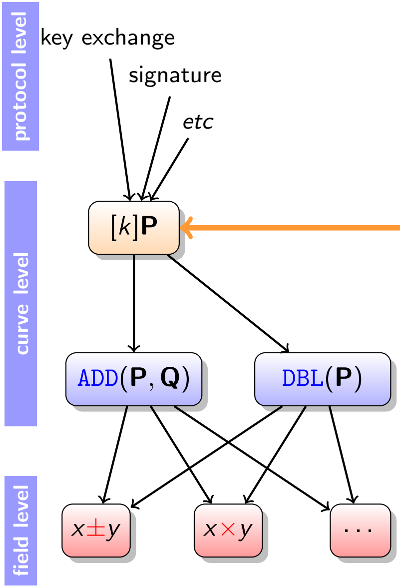

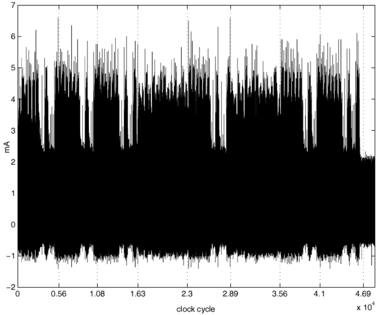

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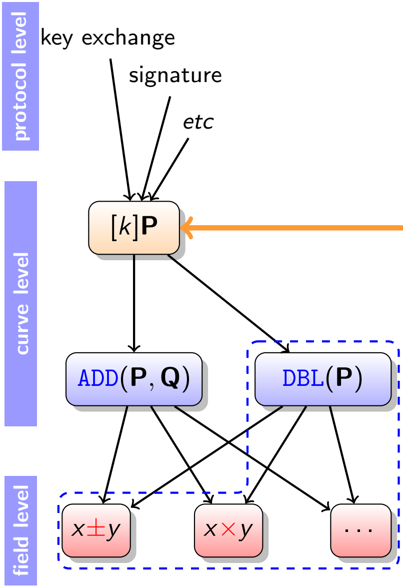

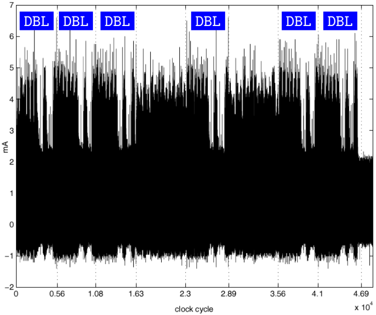

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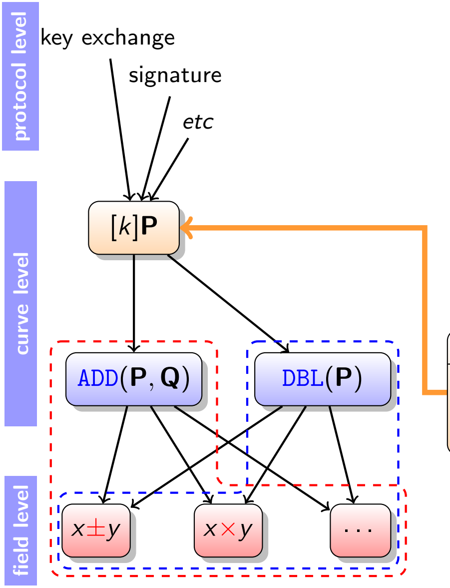

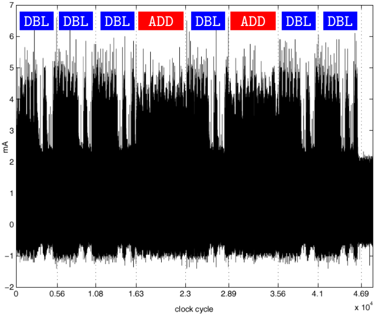

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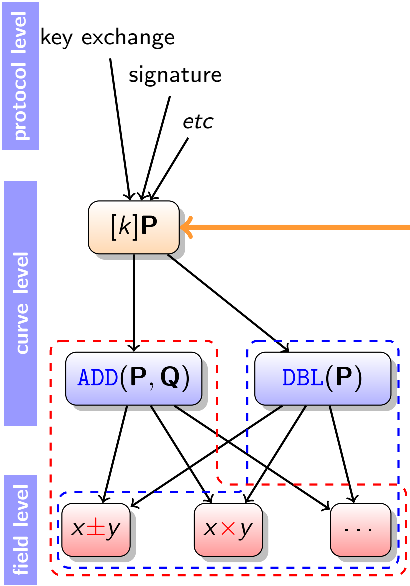

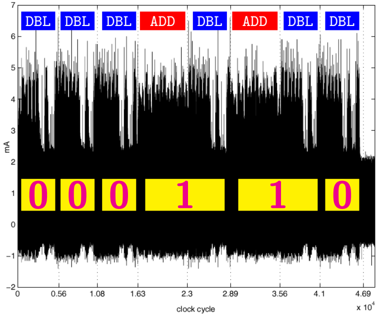

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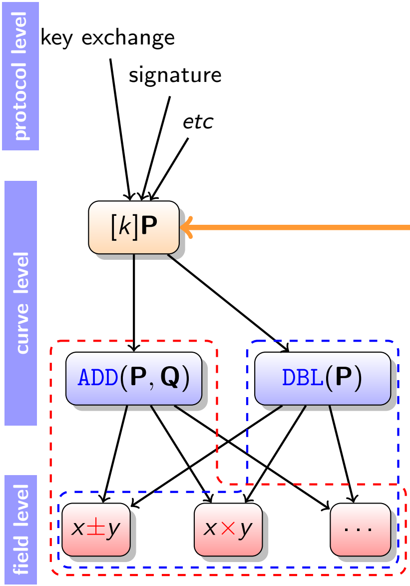

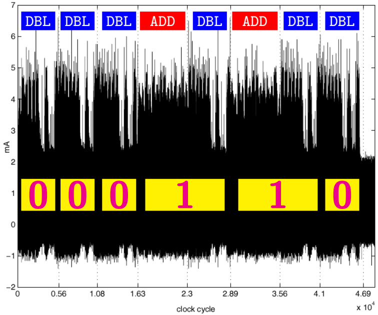

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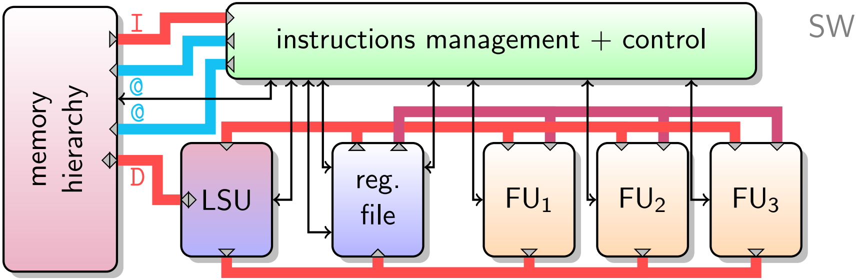
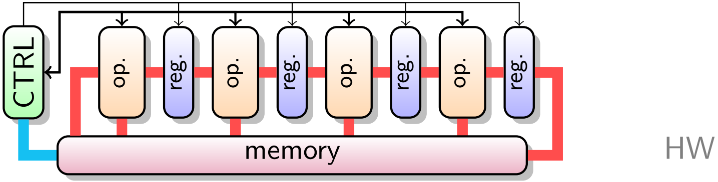
- simple power analysis (& variants)
- differential power analysis (& variants)
- horizontal/vertical/templates/. . . attacks

Software vs Hardware Support



EXCELLENT	slow	large	large	moderate
FLEXIBILITY	SPEED	AREA	ENERGY	DEVEL. COST
limited	fast	small	small	HUGE



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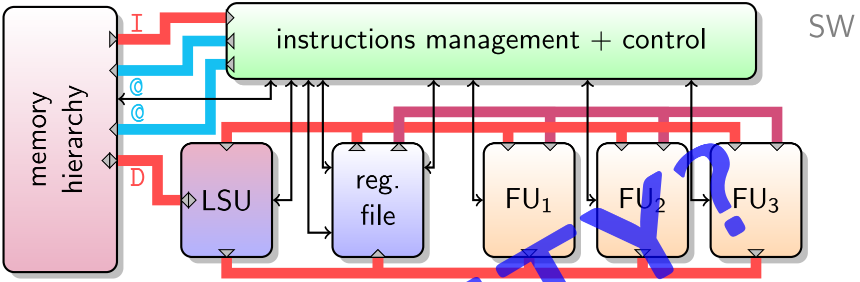

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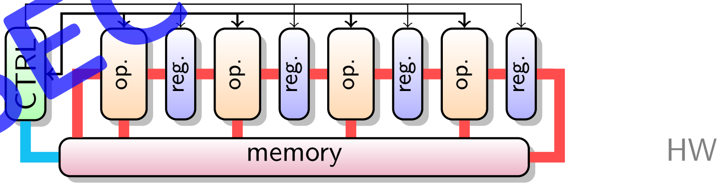
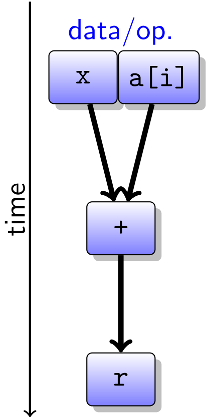


SECURITY?

Activity in a Processor

Operation to be executed: `r ← x + a[i]`



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- PIS: fetch, decode, pipeline management, bypasses, memory hierarchy, branch predictor, monitoring, etc.

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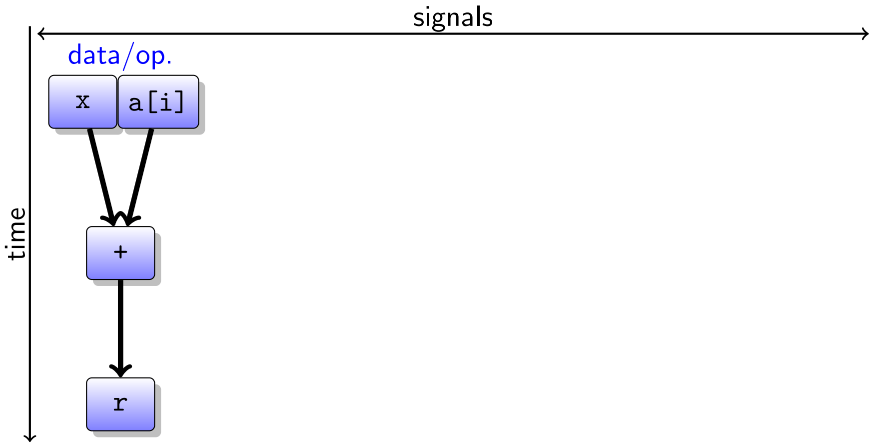

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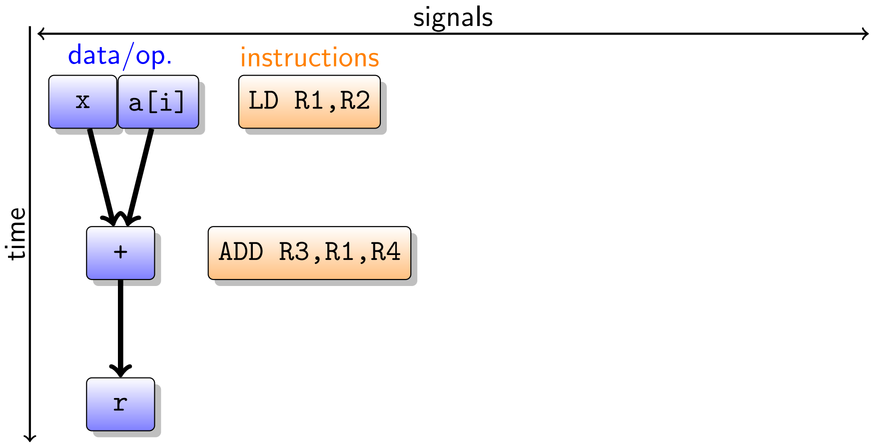

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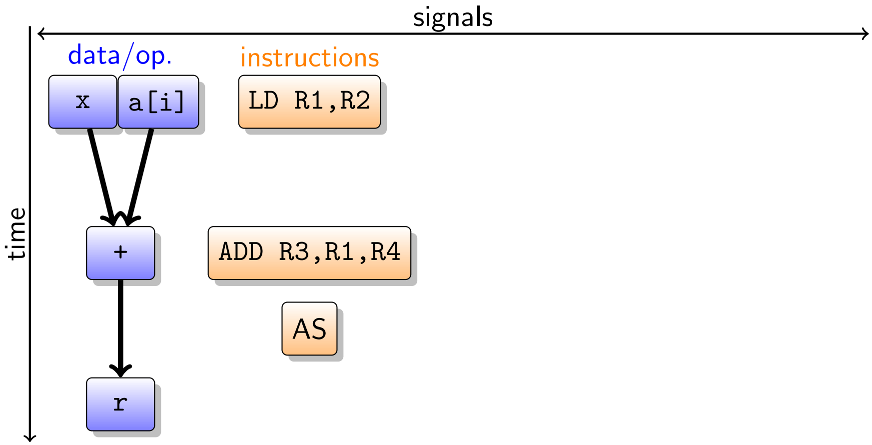

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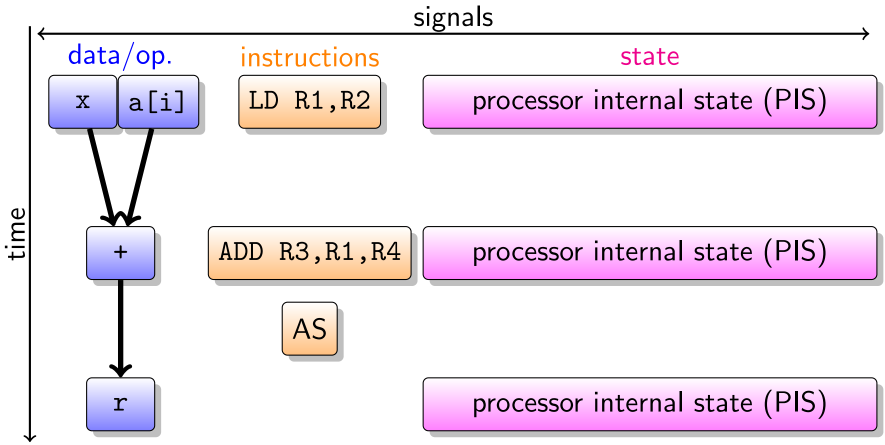

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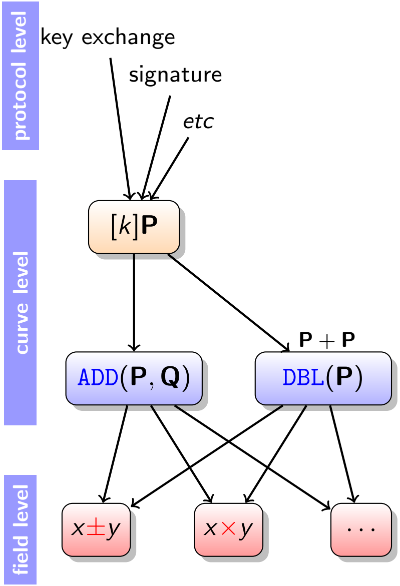
Our Processor Specifications



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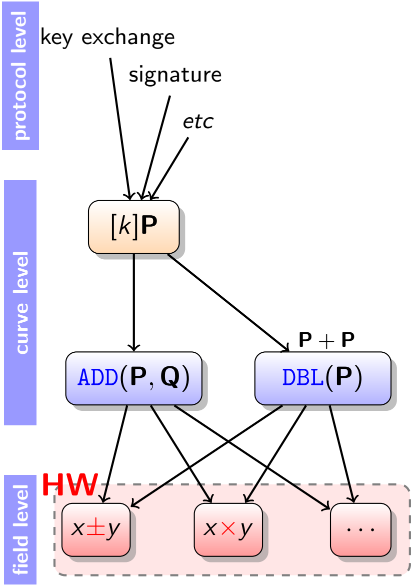

- Performances $\Longrightarrow$ hardware (**HW**)
  - dedicated functional units
  - internal parallelism
- Limited cost (embedded systems)
  - reduced silicon area
  - low energy (& power consumption)
  - large area used at each clock cycle

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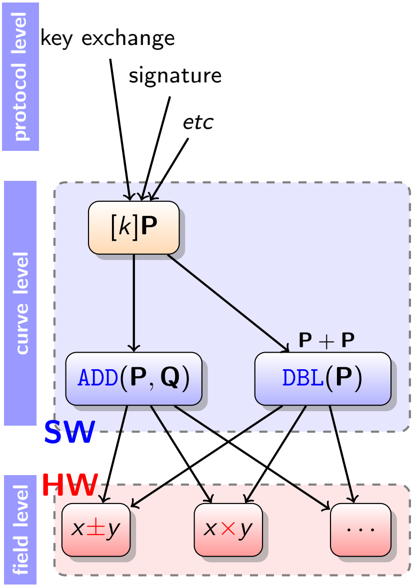

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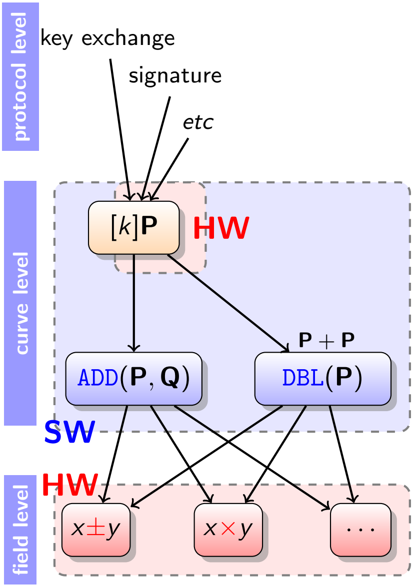

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  - at design time / at run time
- Security against SCAs $\Longrightarrow$ **HW**
  - secure units ($\mathbb{F}_{2^m}$, $\mathbb{F}_p$)
  - secure key storage/management
  - secure control

Processor Architecture

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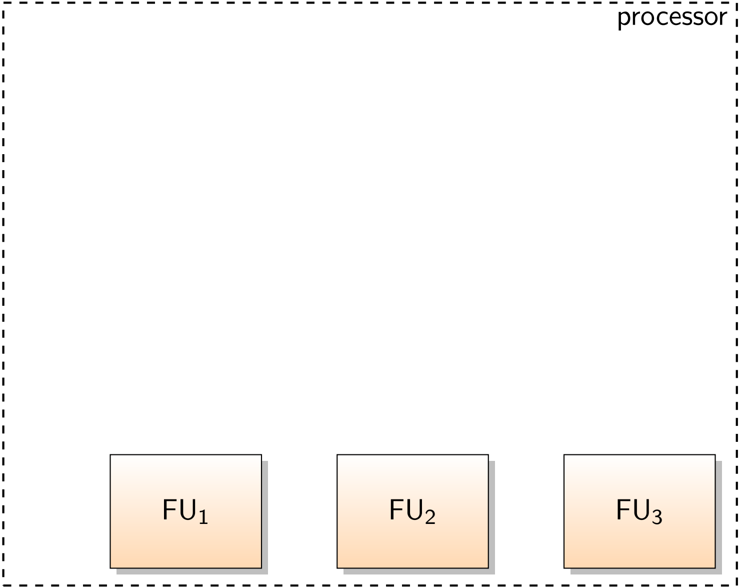

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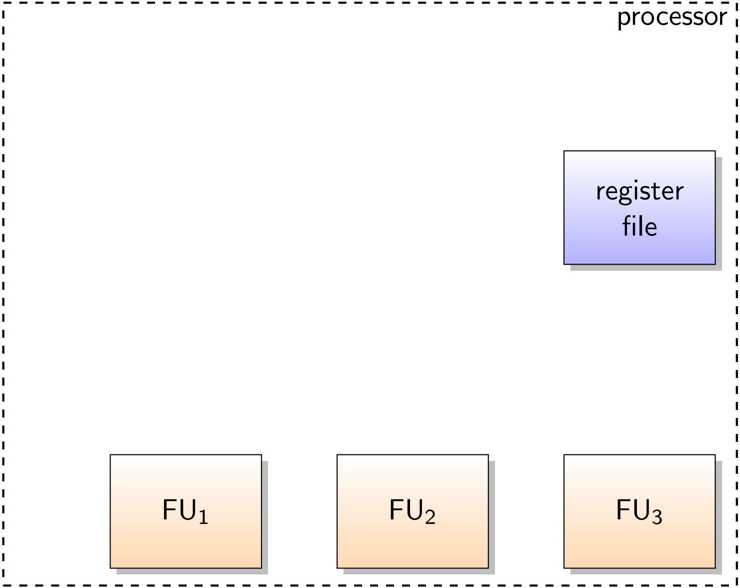

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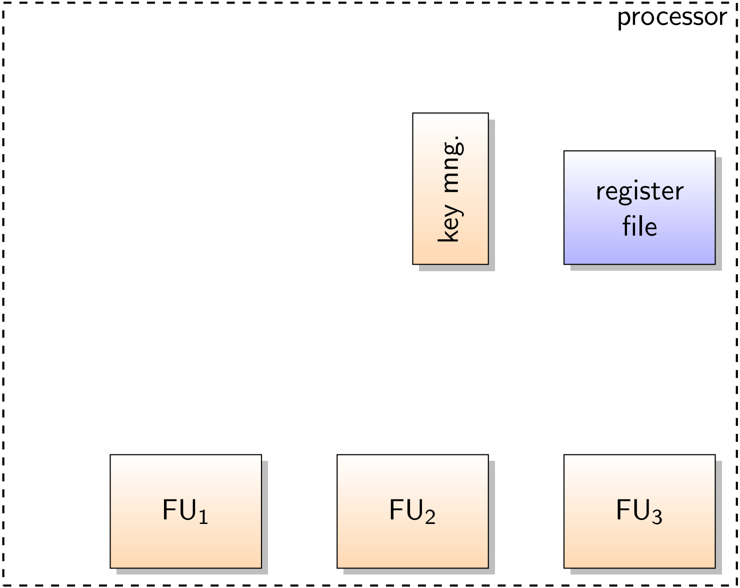

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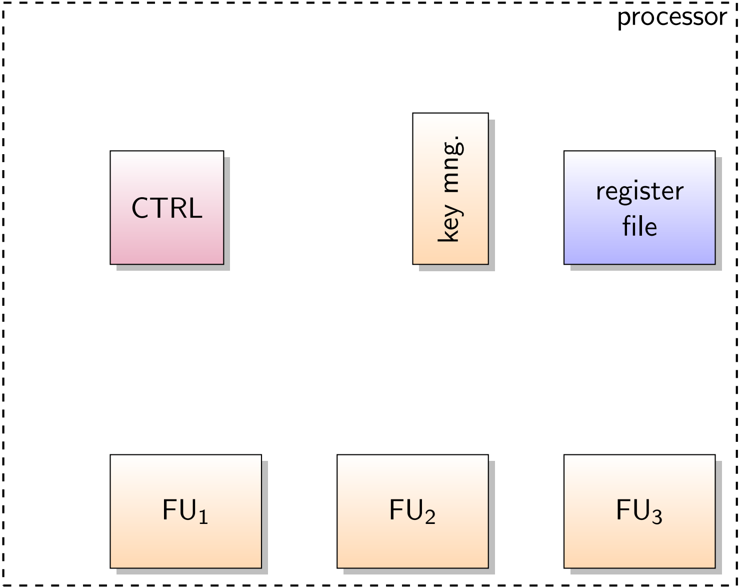

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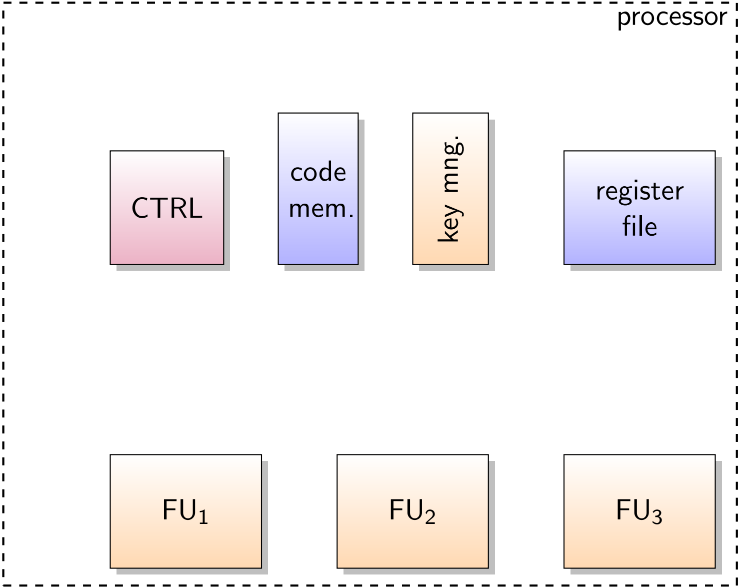

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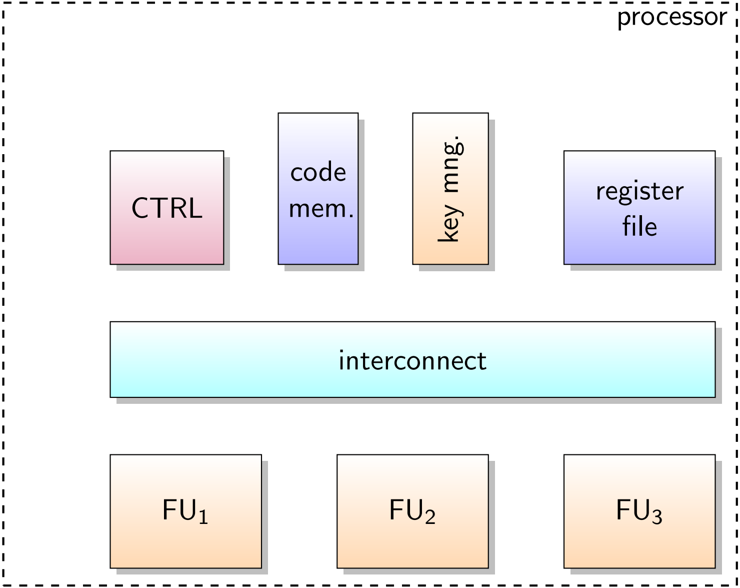

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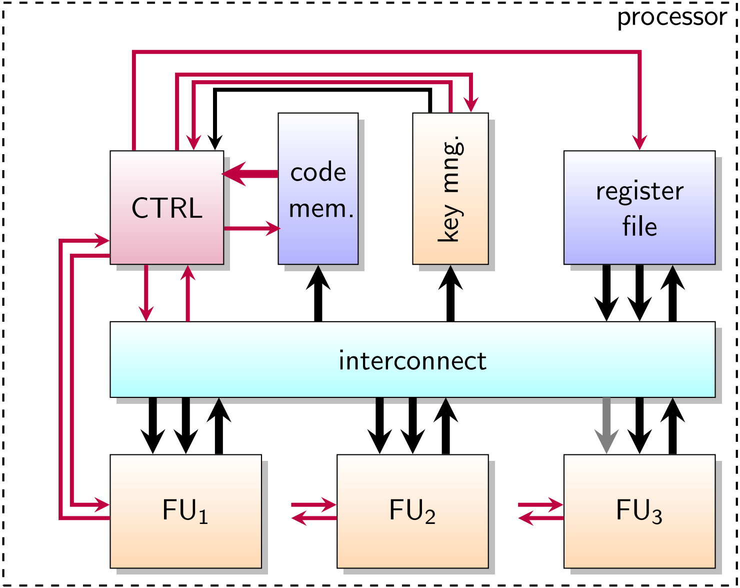

Data: w-bit $(32, \ldots, 128)$ except for k digits, **control**: a few bits per unit

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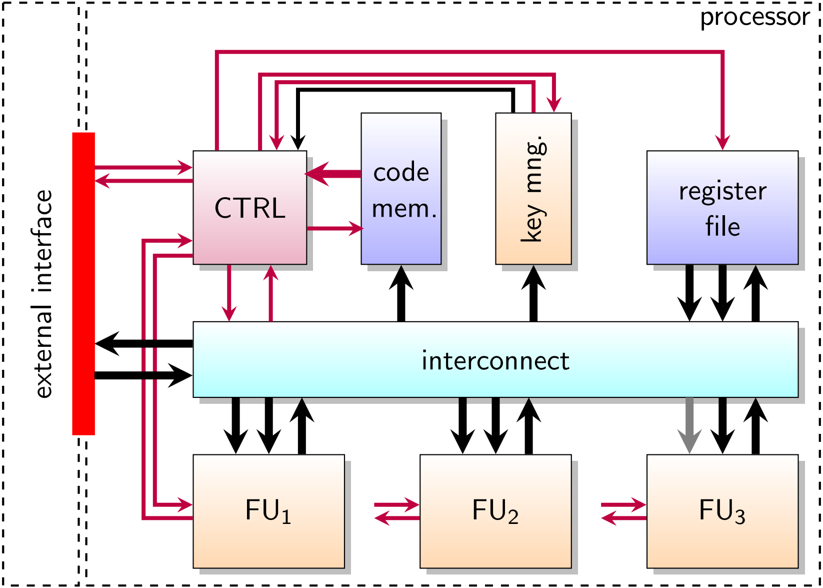

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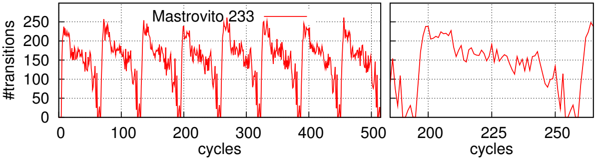
Protected $\mathbb{F}_{2^m}$ Multipliers

Unprotected



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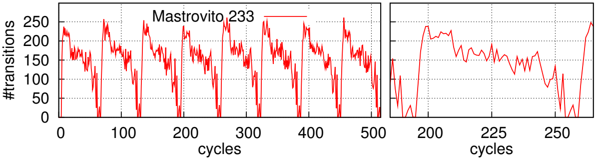
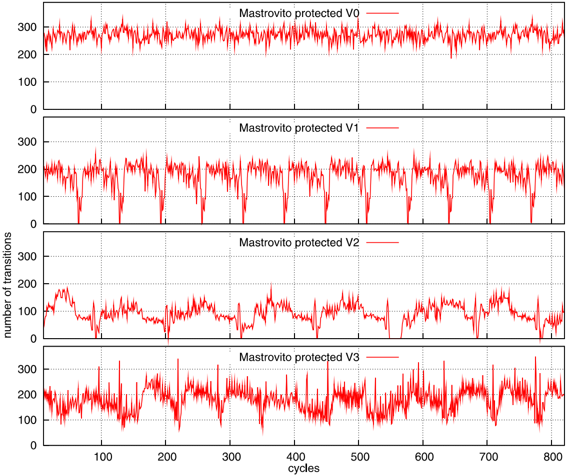


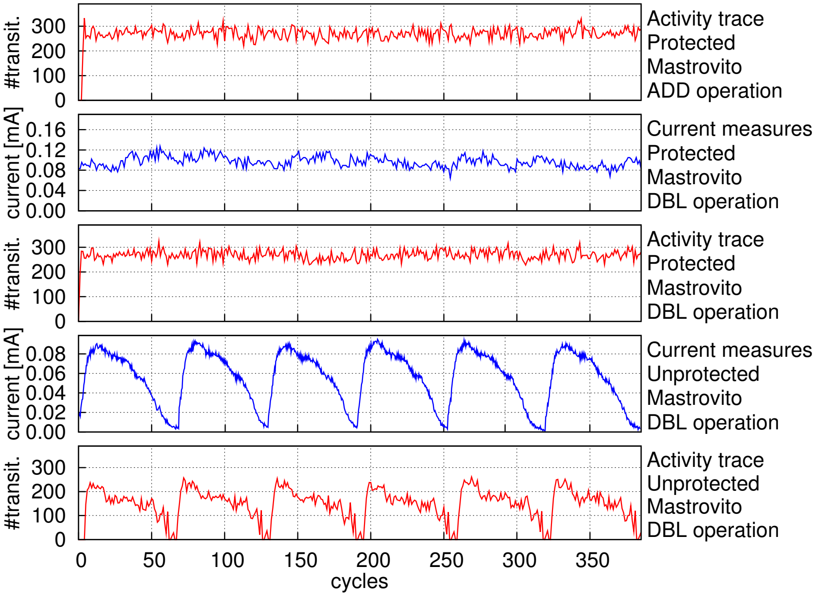
Protected

Overhead:

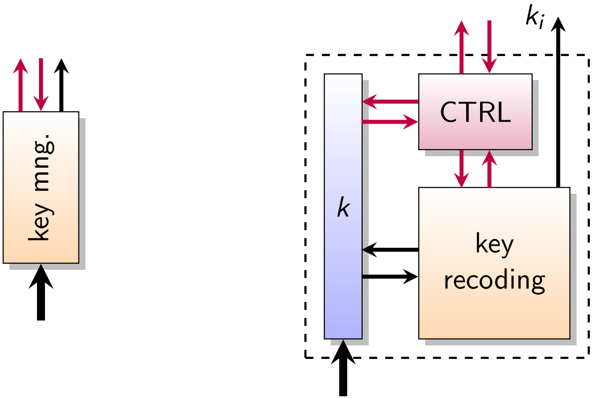
Area/time $< 10\,\%$



Protected Processor for $\mathbb{F}_{2^m}$



Key Management Unit



- On-the-fly recoding of k: binary, λ-NAF ($\lambda \in \{2,3,4,5\}$), variants (fixed/sliding), double-base [6] and multiple-base [7] number systems (w/wo randomization), addition chains [20], other ?
- Specific private path in the interconnect (no key leaks in RF or FUs)

Double-Base Number System

Standard radix-2 representation:

$$k = \sum_{i=0}^{t-1} k_i 2^i = \begin{array}{|c|c|c|c|c|c|}\hline k_{t-1} & k_{t-2} & \cdots & k_2 & k_1 & k_0 \\ \hline \end{array} \; t \text{ explicit digits}$$

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implicit weights

t explicit digits

Digits: $k_i \in \{0, 1\}$, typical size: $t \in \{160, \ldots, 600\}$

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DBNS is a very redundant and sparse representation: $1701 = (11010100101)_2$

$$\begin{aligned} 1701 &= 243 + 1458 = 2^0 3^5 + 2^1 3^6 = (1, 0, 5), (1, 1, 6) \\ &= 1728 - 27 = 2^6 3^3 - 2^0 3^3 = (1, 6, 3), (-1, 0, 3) \\ &= 729 + 972 = 2^0 3^6 + 2^2 3^5 = (1, 0, 6), (1, 2, 5) \\ &\ldots \end{aligned}$$

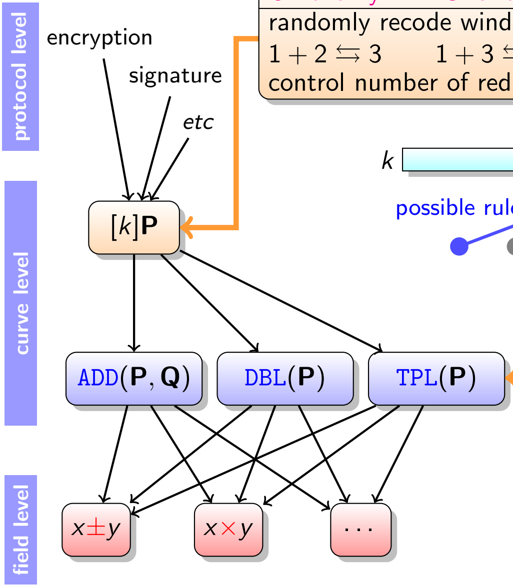
Randomized DBNS Recoding of the Scalar k

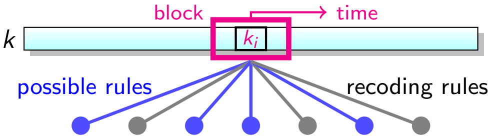
On-the-fly DBNS random recoding for the scalar k

randomly recode windows of the scalar k on-the-fly:

$1+2 \leftrightarrows 3 \qquad 1+3 \leftrightarrows 2^2 \qquad 1+2^3 \leftrightarrows 3^2 \qquad \ldots$

control number of reductions ($\leftarrow$) and expansions ($\rightarrow$)





Point tripling operation

$\mathbf{Q} = \mathtt{TPL}(\mathbf{P}) = \mathbf{P} + \mathbf{P} + \mathbf{P}$

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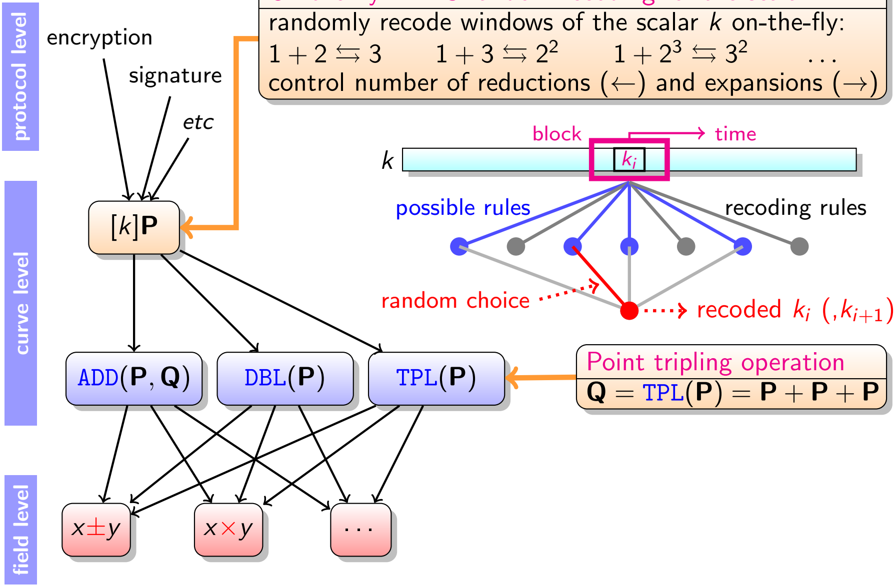


Point tripling operation

$\mathbf{Q} = \mathtt{TPL}(\mathbf{P}) = \mathbf{P} + \mathbf{P} + \mathbf{P}$

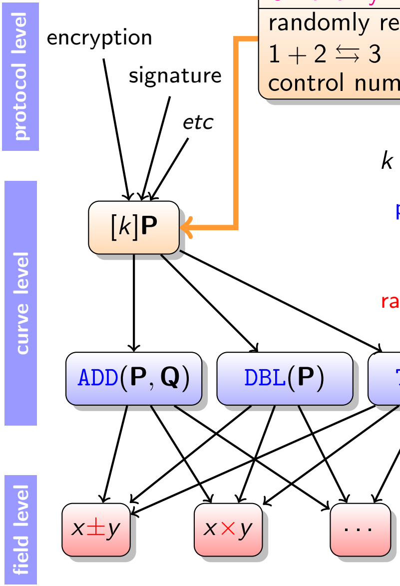
Randomized DBNS Recoding of the Scalar k

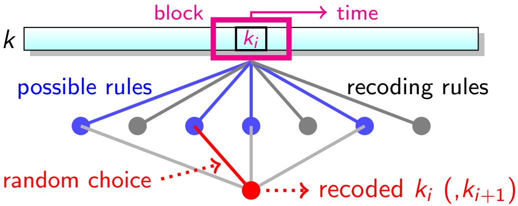
On-the-fly DBNS random recoding for the scalar k

randomly recode windows of the scalar k on-the-fly:

$1 + 2 \leftrightarrows 3 \qquad 1 + 3 \leftrightarrows 2^2 \qquad 1 + 2^3 \leftrightarrows 3^2 \qquad \ldots$

control number of reductions ($\leftarrow$) and expansions ($\rightarrow$)





Point tripling operation

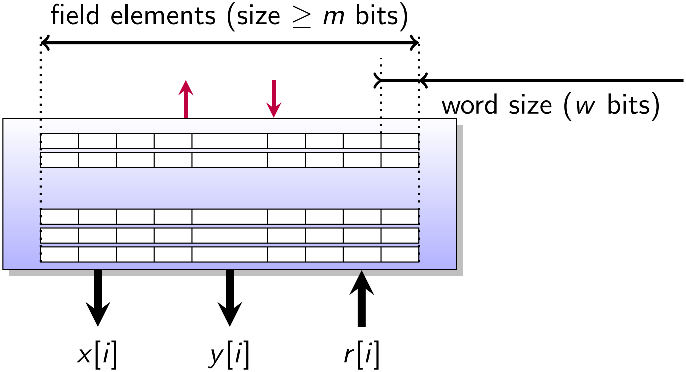
$\mathbf{Q} = \mathtt{TPL}(\mathbf{P}) = \mathbf{P} + \mathbf{P} + \mathbf{P}$

DBNS is redundant $\Rightarrow$ security $\nearrow$

DBNS is sparse $\Rightarrow$ 20–30 % speed $\nearrow$

Ref: [6]

Register File (≈ Dual Port Memory)

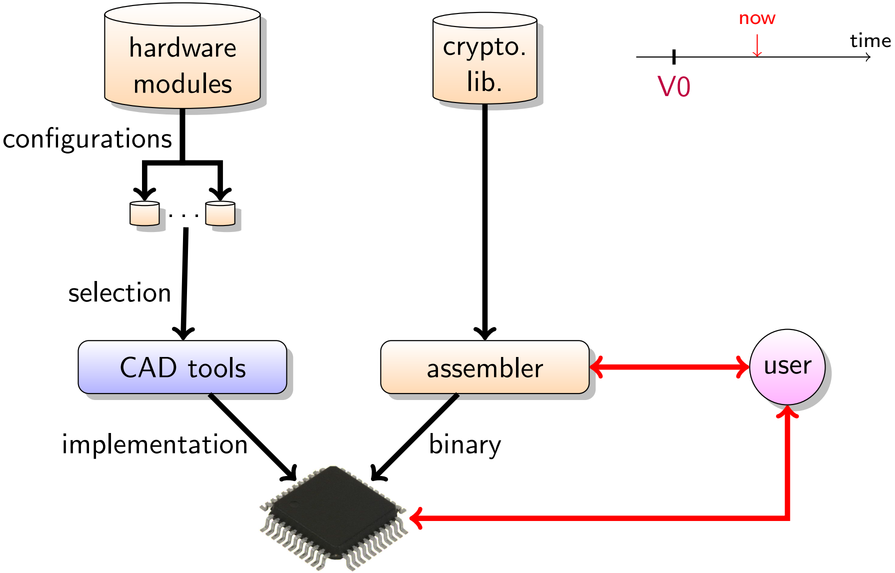


Control signals: addresses (port A, port B), read/write, write enable

Specific addressing model for $\mathbb{F}_q$ elements through an intermediate address table with hardware loop

- linear addresses, SW: `LOAD @`$x \Longrightarrow$ HW: loop $x[0], x[1], \ldots x[\ell - 1]$
- randomized addresses (specific PRNG)

Developed Programming Tools



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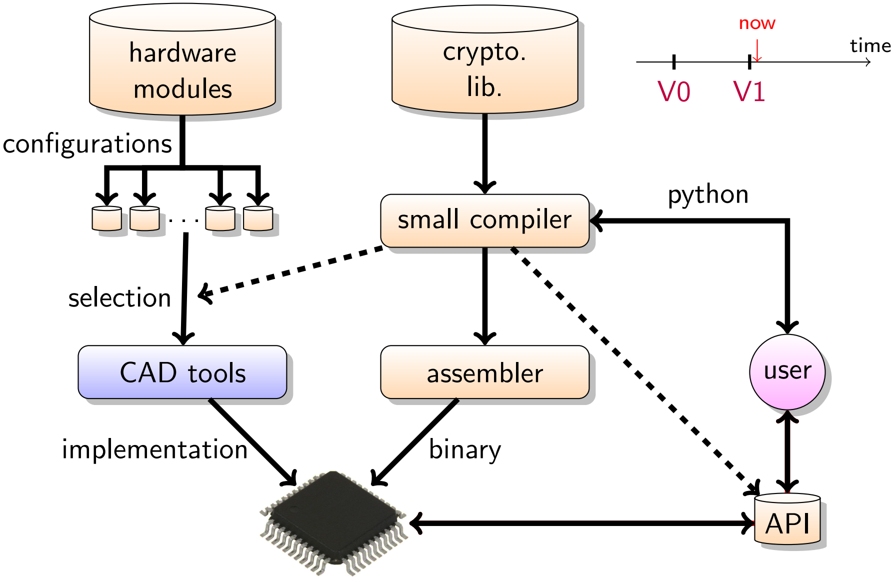

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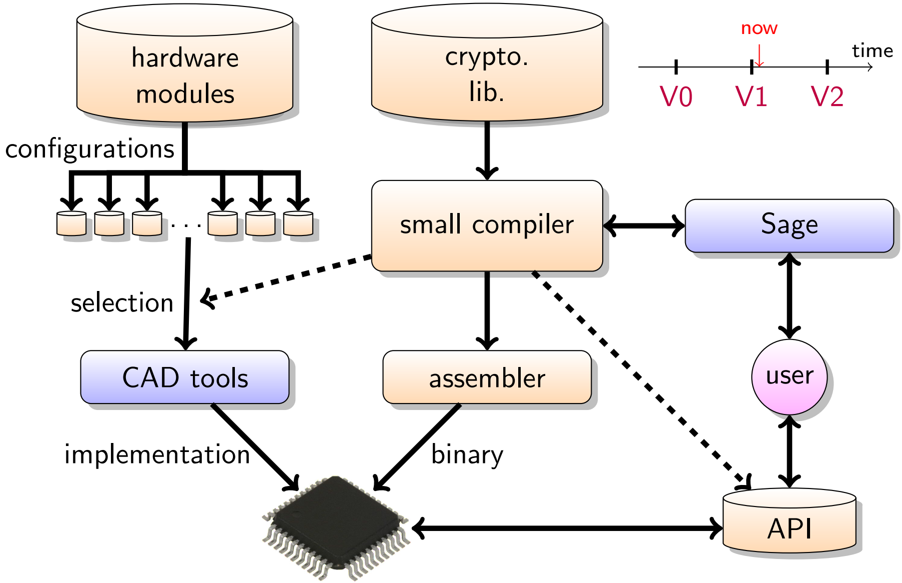
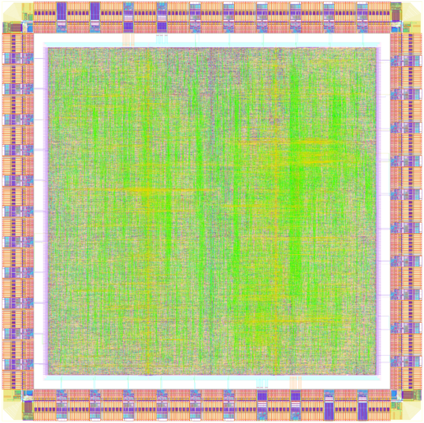
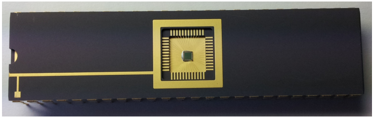


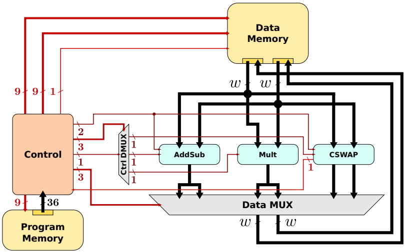
PAVOIS Integrated Circuit

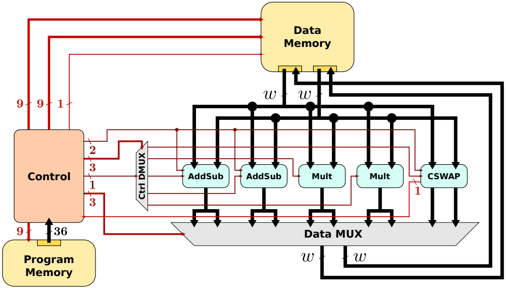


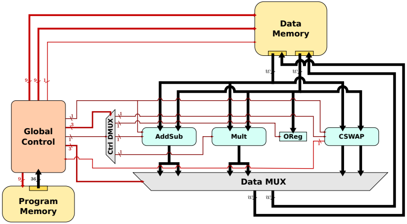
ECC 256 bits
GF(p) with p configurable
65 nm CMOS
1.5 mm^2
algo. & arith. protections
basic layout obfuscation

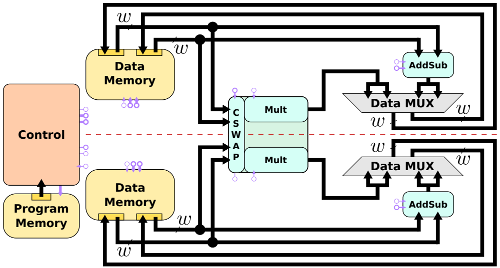


Cryptoprocessors for HECC









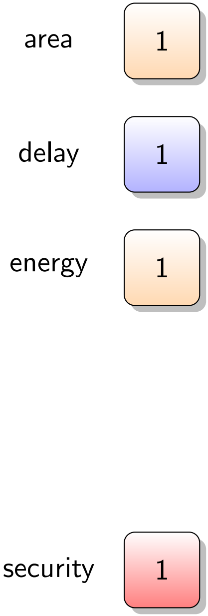
Our Long Term Objectives

Study the links between:

- cryptosystems
- arithmetic algorithms
- $\mathbb{F}_q$, pts representations
- architectures & units
- circuit optimisations

to ensure

- high security against
  - theoretical attacks
  - physical attacks
- low design cost
- low silicon cost
- low energy(/power)
- high performances
- high flexibility



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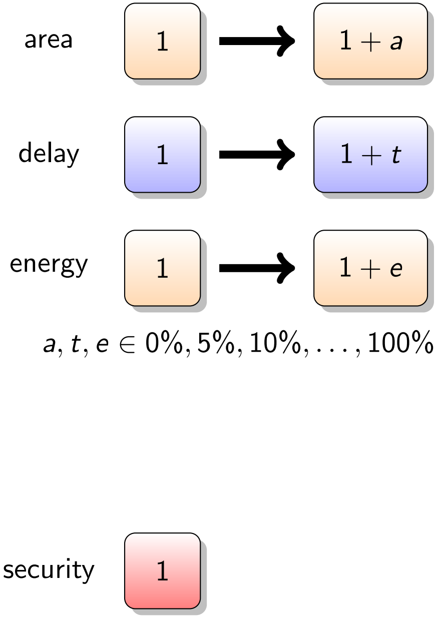

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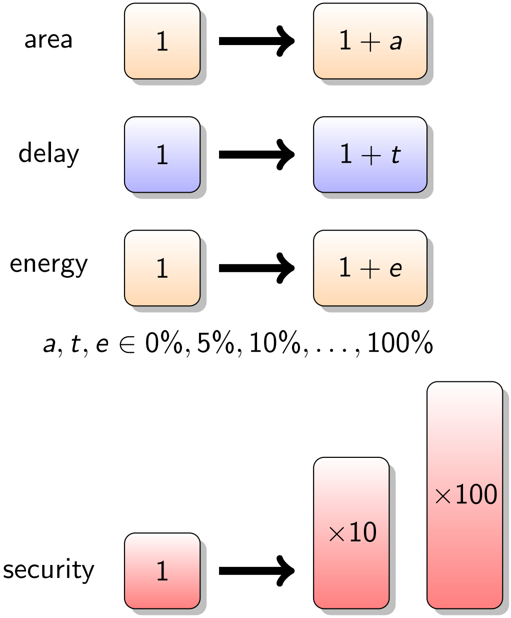

The end, questions ?

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- CNRS
  Lab-STICC, Centre Recherche UBS
  Rue St Maudé. BP 92116. 56321 Lorient cedex, France

Thank you

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